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10/077,947	02/20/2002	Hideki Okuyama	8039-1001	3041

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,947	OKUYAMA, HIDEKI	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 19-36 are presented for examination.

Response to Arguments

2. Applicant's arguments with respect to new claims 19-36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 27 is objected to because of the following informalities: "said other others" (line 3) should be changed to "said other" or "said others" . Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Alaiwan et al. (5,235,700) (hereinafter Alaiwan).

As to claim 19, Alaiwan teaches a multiprocessor system (Fig. 1 and 8) comprising: plurality processors (e.g. processors 12-1, 12-2, and associated circuitry) which send and receive predetermined information to and from each other; and a shared memory (e.g. queues 32-1, 32-2) which shared and accessible by said plurality of

processors one after another, wherein, once each of said plurality of processors has accessed said shared memory, when one of said plurality of processors updates a predetermined data in said shared memory, said one of said plurality of processors requests others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. processor 12-1 issues a READ memory instruction to mirroring control circuit 30-2 in processor 12-2 after a write operation or at appropriate points of working process) (col. 5 lines 7-48).

As to claim 20, Alaiwan further teaches said one of said plurality processors requests others of said plurality of processors to update said updated predetermined data from said shared memory (e.g. when processor 12-1 fails, control signal is sent to processor 12-2) (col. 4 lines 21-60 and col. 5 line 63 to col. 6 line 10).

As to claim 21, Alaiwan further teaches said one of said plurality of processors requests others of said plurality of processors to update the predetermined data in said shared memory, when said others of said plurality of processors have not yet updated said predetermined data (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-24, 26-28, 30-32, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan et al. (5,235,700) (hereinafter Alaiwan) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa).

As to claim 22, Alaiwan teaches a multiprocessor system (Fig. 1 and Fig. 8) comprising: a plurality of processors (12-1,...12-n) which send receive predetermined information to and from each other; a shared memory (e.g. queues 32-1, 32-2) which is shared and accessed by each of said plurality of processors; wherein, once each of said plurality of processors has accessed said shared memory, when said one of said plurality of processors updates a predetermined data said shared memory, said one of said plurality of processors requests others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. processor 12-1 issues a READ memory instruction to mirroring control circuit 30-2 in processor 12-2 after a write operation or at appropriate points of working process) (col. 5 lines 7-48). However, Alaiwan does not explicitly disclose an access manager which manages access to said shared memory by each of said plurality of processors, wherein, when said plurality of processors are in contention to access said shared memory, said access manager selects one of said plurality of processors and permits said one of said plurality of processors to access said shared memory. Ogawa teaches bus handler to manage access contention to a shared memory (2-2) and permit one of the processors to access the shared memory when the processors are in contention (Fig. 3 and col. 9 line 63 to col. 10 line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

As to claim 23, Alaiwan further teaches said one of said plurality of processors requests others of said plurality of processors to update said updated predetermined data from said shared memory (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claim 24, Alaiwan further teaches said one of said plurality of processors requests others of said plurality of processors to update the predetermined data from said shared memory when said others of said plurality of processors have not yet updated said predetermined data (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claim 26, Alaiwan teaches a multiprocessor system comprising: plurality processors (12-1,...12-n) (Fig. 1 and Fig. 8) which send and receive a predetermined signal to and from each other; a shared memory (e.g. queues 32-1, 32-2) which is shared and accessed by each of said plurality of processors; and wherein, once said one of said plurality of processors has accessed said shared memory said one of said plurality of processors outputs an access-request signal to another one of said plurality of processors, so as to request said another one of said plurality of processors to access said shared memory (e.g. processor 12-1 issues a ERP instruction (or READ memory instruction) to mirroring control circuit 30-2 in processor 12-2 after a write operation or at appropriate points of working process) (col. 5 lines 7-48), and wherein once each of said plurality of processors has accessed said shared memory, when said one of said plurality of processors updates a predetermined data in said shared memory, said one of said plurality of processors outputs a re-read request signal to another of said plurality of processors, so as to request said others of said plurality of processors to access said updated predetermined data from said shared memory (e.g. after processor 12-1 updates the

shared memory again (e.g. at the next recovery point), it notifies other processor 12-2 to update the data again, and so on) (col. 5 lines 7-68). However, Alaiwan does not explicitly disclose a contention determiner which detects whether said plurality of processors are in contention to access said shared memory, and permits one of said plurality of processors to access said shared memory. Ogawa teaches bus handler to manage access contention to a shared memory (2-2) and permit one of the processors to access the shared memory when the processors are in contention (Fig. 3 and col. 9 line 63 to col. 10 line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bus handler as taught by Ogawa in the system of Alaiwan to handle access contention between processors and thus improve the system's performance.

As to claim 27, Alaiwan further teaches said one of said plurality of processors outputs an update-request signal, so as to request said others of said plurality of processors to update said updated predetermined data from said shared memory (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claim 28, Alaiwan further teaches said one of said plurality of processors outputs an update-request signal, so as to request said others of said plurality of processors to update the predetermined data in said shared memory, when said others of said plurality of processors have not yet updated said predetermined data (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claim 30, Alaiwan teaches a shared-memory controlling method to be executed in a multiprocessor system including a plurality of processors (12-1,...12-n)

(Fig. 1 and Fig. 8) which send and receive predetermined information to and from each other, a shared memory (e.g. queues 32-1, 32-2) which is shared and accessed by each of said plurality of processors, said method comprising: performing a first access to said shared memory using one processor (writing to queue 32-2 from processor 12-1) (col. 5 lines 7-17); requesting others of said plurality of processors to perform a second access to said shared memory, when said performing the first access to said shared memory has been done (requesting processor 12-2 to access the data); and performing the second access to said shared memory using said others of said plurality of processors (processor 12-2 accesses the data), wherein, once each of said plurality of processors has accessed said shared memory, said one processor updates a predetermined data in said shared memory and requests said others of said plurality processors to access said updated predetermined data from said shared memory (e.g. after processor 12-1 updates the memory again (e.g. at the next recovery point), it notifies other processor 12-2 to update the data again, and so on) (col. 5 lines 7-68). However, Alaiwan does not explicitly disclose selecting one of said plurality of processors, and permitting said one processor to access said shared memory by an access manager, when said plurality of processors are in contention for said shared memory. Ogawa teaches bus handler to manage access contention to a shared memory (2-2) and permit one of the processors to access the shared memory when the processors are in contention (Fig. 3 and col. 9 line 63 to col. 10 line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bus handler as taught by Ogawa in the system of Alaiwan

to handle access contention between processors and thus improve the system's performance.

As to claim 31, Alaiwan further teaches said requesting step includes said one processor requesting others of said plurality of processors to update said updated predetermined data in said shared memory (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claim 32, Alaiwan further teaches said requesting step includes said one processor requesting others of said plurality processors to update the predetermined data in said shared memory (col. 4 lines 21-60 and col. 5 line 7 to col. 6 line 10).

As to claims 34 and 35, Alaiwan teaches a shared-memory controlling method among a plurality of processors (12-1,...12-n) (Fig. 1 and Fig. 8) comprising: performing a first access to said shared memory (e.g. queues 32-1, 32-2) using one processor (writing to queue 32-2 from processor 12-1) (col. 5 lines 7-17); requesting others of said plurality of processors to perform a second access to said shared memory, when the first access has been done (requesting processor 12-2 to access the data); and performing the second access to said shared memory using the others of said plurality of processors (processor 12-2 accesses the data); wherein, once each of said plurality of processors has accessed said shared memory, said one processor updates predetermined data in said shared memory and requests said others of said plurality processors to access said updated predetermined data from said shared memory (e.g. after processor 12-1 updates the memory again (e.g. at the next recovery point), it notifies other processor 12-2 to update the data again, and so on) (col. 5 lines 7-68). However, Alaiwan does not explicitly

disclose selecting one processor of a plurality of processors, and permitting said one processor to access a shared memory shared by the plurality of processors, when the plurality of processors are in contention for the shared memory. Ogawa teaches bus handler to manage access contention to a shared memory (2-2) and permit one of the processors to access the shared memory when the processors are in contention (Fig. 3 and col. 9 line 63 to col. 10 line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bus handler as taught by Ogawa in the system of Alaiwan to handle access contention between processors and thus improve the system's performance.

6. Claims 25, 29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan et al. (5,235,700) (hereinafter Alaiwan) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa), and further in view of Hauck et al. (6,587,904) (hereinafter Hauck).

As to claims 25, 29, and 33, the arguments above for claims 22, 26, and 30 apply. However, Alaiwan and Ogawa do not explicitly disclose when predetermined period time has elapsed without being selected by said access manager, said one of said plurality of processors requests others of said plurality of processors and said access manager to perform predetermined reset operation for resetting themselves. Hauck teaches detecting if arbitration is not won within a specified amount of time and requesting a long bus reset (at least col. 8, lines 56-67 and col. 12, lines 8-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include detecting if arbitration is not won within a specified amount of time and requesting a long bus reset as

taught by Hauck by each of the plurality of processors in the system of Alaiwan and Ogawa to allow reconfiguration of the bus and connected devices to better provide the actual status of the system.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alaiwan et al. (5,235,700) (hereinafter Alaiwan) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa), and further in view of Mogul (6,704,798).

As to claim 36, Alaiwan teaches a method for controlling a computer to execute a shared-memory controlling among a plurality of processors (12-1,...12-n) (Fig. 1 and Fig. 8) comprising: performing a first access to said shared memory using one processor (writing to queue 32-2 from processor 12-1) (col. 5 lines 7-17); requesting others of said plurality of processors to perform second access to said shared memory, when the first access has been done (requesting processor 12-2 to access the data); and performing the second access using the others of said plurality of processors (processor 12-2 accesses the data); wherein, once each of said plurality of processors has accessed said shared memory, when said one processor updates predetermined data in said shared memory in performing the first access, said one processor requests said others of said plurality of processors to access said updated predetermined data from said shared memory (col. 5 lines 7-68). However, Alaiwan does not explicitly disclose selecting one processor of a plurality of processors, and permitting said one processor to access a shared memory shared by the plurality of processors, when the plurality of processors are in contention for the shared memory. Ogawa teaches bus handler to manage access contention to a

shared memory (2-2) and permit one of the processors to access the shared memory when the processors are in contention (Fig. 3 and col. 9 line 63 to col. 10 line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bus handler as taught by Ogawa in the system of Alaiwan to handle access contention between processors and thus improve the system's performance. However, Alaiwan and Ogawa do not explicitly disclose the method is contained within a data signal embedded in a carrier wave representing an instruction sequence. Mogul teaches implementing a data signal embedded in a carrier wave representing an instruction sequence (col. 14, lines 4-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method via a data signal embedded in a carrier wave representing an instruction sequence as taught by Mogul in the system of Alaiwan and Ogawa to allow the method to be stored and executed in a distributed fashion over the network.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses multiprocessor data processing:

US Patent	5,983,359	Nota et al.
US Patent	5,737,514	Stiffler
US Patent	6,035,417	Kanazawa
US Patent	6,609,214	Dahlen et al.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu
Examiner
Art Unit 2112

uv

TIM VO
PRIMARY EXAMINER